

# COMMUNICATION SYSTEM

This application claims a priority based on Japanese Patent Application No. 2000-20657 filed on January 28, 2000, the entire contents of which are incorporated herein by reference for all purposes.

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a communication system and, more particularly, to a radio communication system based on the code division multiple access system.

### Background of the Invention

A radio communication system employing the code division multiple access method has characteristics suitable for mobile communication, i.e., its strength against mutual interference with other systems, its adaptability to a multipath, capability of easy hand-off, excellent secrecy and so on. However, a communication system based on the code division multiple access method is different from other multiple access methods in that a plurality of terminal users existing within the same base station cell simultaneously communicate using the same frequency and the same frequency band. Therefore, a communication system based on the code division multiple access method has the following problem in utilization of a channel. Specifically, the problem is that utilization

of a channel can be reduced by interference that occurs when a strong communication signal from a user closer to a base station overlaps another weaker signal in the existence of the far-and-near problem, and interference by one station with another station that is caused by unnecessary transmission power from the first station and so on.

Measures to prevent any reduction of utilization of a channel includes the use of a wide band gain through expansion of the band of a signal, the use of a series of codes having little correlation and the use of power control for solving the far-and-near problem. In particular, power control is effective not only in suppressing unnecessary transmission from a station to limit the transmission power of the station to a required minimum thereby minimizing interference of the station with another station but also in solving the far-and-near problem.

However, even when those measures are taken, it is still difficult to prevent any reduction of the quality of communication resulting from an increase in mutual correlation interference (a reduction in a signal-to-noise ratio) attributable to an increase in the number of users who communicate simultaneously.

An effective measure to solve the above-described problem is interference canceling techniques for eliminating interference from another channel, and various types of interference canceling techniques are being

studied. A receiver can predict interference of another user, and the receiver can perform a process to eliminate the interference. Those proposed interference canceling systems include an interference canceling system based on  
5 a multi-user reception method which utilizes information of a plurality of user signals to be demodulated from a plurality of users. An interference canceling apparatus utilizing this system performs a demodulation process on signals to be demodulated from a plurality of users,  
10 performs a re-spreading process and a synthetic process on the demodulated signals to create replica signals, and performs a subtraction process between the replica signals and multi-wave reception signals to realize a demodulation process which suppresses interference components. The  
15 effect of suppressing interference components is improved by performing the interference canceling process using a cascade-connected multi-stage configuration.

For information on interference cancellation of this type, for example, the techniques disclosed in Japanese  
20 patent Laid-Open No. 51353/1998 and 190494/1998 are well known.

#### SUMMARY OF THE INVENTION

In a mobile communication system utilizing code division multiple access as described above, an increase  
25 in mutual interference inevitably occurs as a result of an increase in the number of users who simultaneously

communicat Therefore, interfere cancellation techniques are indispensable techniques. Among such interference cancellation techniques, multi-user reception type interference cancellation techniques  
 5 require a signal processing unit for performing a process of suppressing interference components including a plurality of correlators and re-spreaders because they utilize information of a plurality of user signals to be demodulated. The signal processing unit for performing a  
 10 process of suppressing interference components has a large size and involves a large scale of signal processing because it has a multi-stage configuration for improving the effect of canceling interference components. As a result, a communication system utilizing such an interference  
 15 cancellation method needs an apparatus of a large scale is required at a base station, thereby increasing cost.

It is an object of the invention to provide a communication system utilizing code division multiple access in which any increase in the scale of an apparatus  
 20 at a base transceiver station in simultaneous communication with a plurality of radio mobile station apparatuses is prevented by providing an interference suppressing function for suppressing mutual interference attributable to an increase in the number of users of the communication.

25 It is another object of the invention to provide a low-cost communication system utilizing code division

multiple access which enables prevention of any reduction of channel utilization communication with high quality.

In order to achieve the above objects according to the present invention, there is provided a base transceiver station for use in communication with a plurality of radio mobile station apparatuses based on code division multiple access. The base transceiver station comprises a reception signal interference canceller device. Further, the interference canceller device comprises: a slot configuration circuit for dividing a reception signal at certain time intervals, converting the divided signal into signals at a faster cycle and converting into a signal having a serial slot configuration as many the converted signals as stages for stage processing on a signal identical to the converted signals at a faster cycle; a correlation circuit for performing a despreading process on the signal having the slot configuration; a stage addition circuit for adding the number of stages for stage processing to the despread signals; a re-spreading circuit for performing a re-spreading process on the signals which have been subjected to the stage addition; a synthesis circuit for performing a process of synthesizing all of the spread signals which have been subjected to the re-spreading process to generate replica signals; and a subtraction process circuit for performing a subtraction process between the replica

signal and the reception signals. The base transceiver station, signals obtained by subtraction process for the replica signals and the reception signals are repeatedly fed back to the correlation circuit thereby to eliminate  
5 an interference component.

Further, the above objects can be achieved by dividing the reception signal at certain time intervals at the slot configuration circuit such that one of the divided signals partially overlaps another divided signal at a signal  
10 dividing point. The above objects can be achieved, with respect to the slot signal to be despread among the signals having a serial slot configuration, by allowing only a first slot to pass through and disallowing the rest of the slots to pass through before being inputted to the correlation  
15 circuit, and inputting into the correlation circuit the signal whose second slot and subsequent slots are subjected to an interference cancellation process and fed back.

Moreover, in order to achieve the above objects, there is provided the stage addition circuit which selects valid  
20 signals out of the despread signals inputted thereto, selects signals to be added, and selects signals to be re-spread, and further selects the despread signals for controlling the above selections and adding.

Furthermore, in order to achieve the above objects,  
25 there is provided the correlation circuit which comprises a shift register, despread code setting elements and a

matched filter having an addition circuit. In correlation  
detection for outputting a correlation value signal by  
sequentially shifting the reception signals inputted to the  
shift register to the subsequent stages, and meanwhile  
5 integrating with the despread code setting elements, and  
adding the integrated signals, the matched filter conducts  
correlation detection by switching despread codes set in  
the despread code setting element within the period during  
which the signals in the shift register are shifted to the  
10 subsequent stages, and performs a despreading process for  
a plurality of users.

In addition, in order to achieve the above object of  
the present invention, there is provided the path detection  
circuit which comprises: a selector for selecting pilot  
15 signal portions at the beginning of the correlation value  
signals outputted by the correlation circuit; an averaging  
circuit for performing an averaging process on the selected  
pilot signals among the slot signals; an accumulation  
circuit for performing accumulation of the averaged pilot  
20 signals and the slot signals in the subsequent stages; a  
forgetful averaging circuit for performing a forgetful  
averaging process between the accumulatively added signals  
and other accumulatively added signals in the subsequent  
stages; a path detection/peak detection circuit for  
25 detecting paths for the reception signals from the  
correlation value signals which have been subjected to the

forgetful averaging process and detecting the peaks and  
positions of valid paths; and a despread signal detection  
circuit for detecting despread signals from the correlation  
value signals based on the information of valid paths  
5 detected by the path detection/peak detection circuit.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of  
a communication system utilizing code division multiple  
10 access according to an embodiment of the invention.

Fig. 2 is a block diagram showing a configuration of  
a base transceiver station apparatus having an interference  
canceller device.

Fig. 3 is a block diagram showing a configuration of  
15 the interference canceller device.

Fig. 4 illustrates conversion of a reception signal  
into a signal having a slot configuration by a slot  
configuration circuit.

Figs. 5A through 5C illustrate a method of allocating  
20 signals during a process at stages for canceling  
interference between slot configuration signals.

Figs. 6A and 6B illustrate a configuration of a stage  
process circuit and a process of adding despread signals  
at the same circuit.

25 Fig. 7 is a block diagram illustrating a configuration  
of a correlation circuit of the interference-canceling



device.

Fig. 8 is a block diagram illustrating a configuration of a path detection circuit of the interference-canceling device.

5 Fig. 9 is a process flow for eliminating interference component.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

10 An embodiment of a communication system according to the invention will now be described in detail with reference to the drawings.

Fig. 1 is a block diagram showing a configuration of a communication system utilizing code division multiple access according to an embodiment of the invention. Fig. 15 2 is a block diagram showing a configuration of a base transceiver station apparatus having an interference-canceling device. First, a schematic description will be made on configurations of the communication system and base transceiver station of the present embodiment. In Figs. 20 1 and 2, 11 represents a mobile station (MS); 12 represents a base transceiver station (BTS); 13 represents a base station controller (BSC); 14 represents a mobile switching center(MSC); 15 represents a public switched telephone network; 20 represents an antenna unit; 21 represents a 25 transmit-receive amplifier; 22 represents a radio transmitter receiver; 23 represents a baseband processor;

24 represents a hard wired interface unit; and 25 represents a base transceiver station controller.

As shown in Fig. 1, the mobile communication system to which the invention applied includes the mobile station apparatuses 11, the base transceiver station apparatus 12 which communicates with a plurality of the mobile stations 11 utilizing the code division multiple access method, the base station controller 13 which is connected to a plurality of the base transceiver station 12 to perform processes of selecting, synthesizing and distributing communication signals and control signals to perform a diversity hand-over process to the mobile stations 11 and the mobile switching center 14 which is connected to a plurality of the base station controllers 13 and other communication apparatuses to perform a process of exchanging communication signals, the system being connected to the public switched telephone network 15.

The base transceiver station apparatus 12 employs the code division multiple access method as its communication method and communicates with a plurality of radio mobile station apparatuses 11 existing within a radio area of the base transceiver station apparatus 12. A plurality of the base transceiver station apparatuses 12 which are mobile terminal users communicate using the same frequency and frequency band. Since each communication uses a different code, each communication is performed on a divided basis.

Processes such as power control are performed at the base transceiver station apparatuses in order to solve the far-and-near problem that occurs when a strong communication signal from a mobile terminal user located close to a base transceiver station apparatus 12 overlaps a weaker communication signal from a mobile terminal user located further.

The base station controller 13 is connected to a plurality of the base transceiver station apparatuses 12. The base station controller 13 performs a process of selecting and synthesizing communication signals and control signals from each of the base transceiver station apparatus 12 and a process of distributing communication signals and control signals to each base transceiver station apparatus 12. The base station controller 13 also performs a diversity hand-over process for switching communication signals between base transceiver station apparatuses when a radio mobile station apparatus 12 moves from a radio area covered by one base transceiver station apparatus 12 to another radio area covered by another base transceiver station apparatus.

As shown in Fig. 2, the base transceiver station apparatus 12 comprises an antenna unit 20, a transmit-receive amplifier 21, a radio unit 22, a baseband processor 23, a hard wired interface unit 24 and a base transceiver station control unit 25.



portion and a baseband reception portion. The baseband transmission portion performs signal processing such as transformation of transmission data into error correction codes, framing, data modulation and spread modulation. The baseband reception portion has an interference canceller device 23a and performs signal processing such as synchronization of reception of signals from the radio unit 22, despreading, an interference suppressing process, decoding of error correction codes, multiplex division of data, synthesis of sectors at a maximum ratio during diversity hand-over.

The hard wired interface unit 24 is an interface unit for an inter-station transmission channel between the base transceiver station apparatus 12 and the base station controller 13. The hard wired interface unit 24 transmits and receives communication signals to and from the base station controller 13.

The base transceiver station control unit 25 transmits and receives control signals to and from the base station controller 13 and performs processes such as management, setting and opening of radio lines.

A detailed configuration and operation of the interference canceller device 23a in the base transceiver station apparatus 12 will now be described with reference to the drawings.

In Fig. 3 and Figs. 6 through 8, 101 represents a



reflect the result of the path detection upon the division  
of a signal, the slot signal configuration circuit 103 for  
dividing at certain time intervals a reception signal for  
which path detection has been performed to convert the  
5 signal into signals having a slot configuration, the  
selector 104 for selecting the slot signals, the correlation  
circuit 105 for performing a despreading process on the  
signals having a slot configuration, the path detection  
circuit 106 for detecting a path for an interference  
10 suppression signal; the stage addition circuit 115 for  
adding the number of stages of stage processing to a despread  
signal on which has been subjected to the despreading  
process, the re-spreading circuit 110 for performing a  
process of re-spreading the signal which has been subjected  
15 to the stage addition, the synthesis circuit 111 for  
performing a synthetic process on all signals which have  
been subjected to the re-spreading process to generate  
replica signals, the subtraction process circuit 112 for  
performing a process of subtracting the replica signals as  
20 a result of the synthetic process from reception signals,  
the code generation circuit 108 for generating codes for  
the despreading and re-spreading processes, the selectors  
107 and 109 for switching those codes and the demodulation  
circuit 116 for performing a demodulation process on signals  
25 on which interference cancellation has been performed.

A reception signal inputted to the interference

cancellation device 23a is a reception signal which has been subjected to the synchronization process and path detection on a multi-wave signal which has been received by the radio unit 22. The slot signal configuration circuit 103 divides the reception signal at certain time intervals to convert it into signals at a faster cycle and further converts them into signals having a serial slot configuration. The signals configured into slots have a configuration in which the signals equal to the divided signals are located repeatedly. Some of the signals having a slot configuration are inputted to the subtraction processing unit 112 through the delay circuit 113 as they are in the slot configuration in which the signals are located repeatedly. The rest of the signals having a slot configuration are inputted to the selector 104. The selector 104 performs a process of allowing only the signal in the first slot to pass therethrough and disallowing the remaining slots to pass therethrough. The signals processed by the selector 104 are input to the subsequent processing circuit for performing the interference cancellation process.

The signals only whose first slots have passed are inputted to the correlation circuit 105 for performing the despreading process. The correlation circuit 105 performs the process of the correlation detection process and re-spreading process on the multiplex input signals in a number of times equivalent to the number of users. The



despread signals are inputted to the re-spreading circuit 110, as they are in the slot configuration, through the path detection circuit 106 and stage processing circuit 115. After the re-spreading circuit 110 generates re-spread signals, the synthesis circuit 111 synthesizes the re-spread signals of all of the users to generate replica signals. The replica signals are inputted to the subtraction process circuit 112. At the subtraction process circuit 112, a subtraction process is performed between the replica signals and the signals having the slot configuration of repeated signals input from the delay circuit 113. The signals resulting from the subtraction process are fed back to the correlation circuit 105 through the delay circuit 114 and the selector 104.

15 A despreading process is similarly performed on the signals fed back to the correlation circuit 105 which have been subjected to the subtraction process. For example, the feedback to the correlation circuit 105 is carried out at timing of which the signal in the first slot becomes the signal in the second slot if it is processed and fed back. 20 Therefore, the interference canceller device 23a can process the signals continuously. A re-spreading process and a synthesis process similar to those described above are performed also on the signal in the second slot which has been fed back and subjected to the despreading process. 25 This replica signal is also

fed back to the correlation circuit 105 after being subjected to the subtraction process as described above. The fed back signal becomes the signal in the third slot. As thus described, the interference canceller device 23a performs the same process repeatedly to achieve a multi-stage type interference canceling function. This makes it possible to improve the effect of suppressing interference components.

As described above, the process at the multi-stage interference canceller of the present embodiment utilizes signals having a serial slot configuration which are generated by dividing a reception signal at certain time intervals. The signals converted into a slot configuration are subjected to the despreading process at the correlation circuit. The signals in a slot configuration are discrete signals because they are obtained by dividing a continuous signal into slots. Therefore, if the divided signals are located in slots as they are, the correlation circuit is unable to perform the demodulation process at the discontinuities. Under such circumstances, according to the present embodiment, the slot configuration circuit 103 performs the process described below in order to allow the correlation circuit to perform demodulation in the same way as performed on a continuous signal even at the discontinuities.

A description will now be with reference to Fig. 4 on

how a reception signal is converted by the slot configuration circuit 103 into signals in a slot configuration.

5 The received signal is a signal, from a 10 of subscribers of radio mobile station apparatuses 11, which has been subjected to code division multiplexing. The slot configuration circuit 103 divides such a reception signal 201 at certain time intervals which are arbitrarily set to convert it into signals having a faster cycle and thereafter  
10 converts the resultant signals into signals in a serial slot configuration. Such signal conversion is performed such that the above-described signals divided at certain time intervals are arranged as m similar signals at a higher speed at the same time intervals as described above to provide  
15 signals 202 having a slot configuration.

Since the reception signal 201 is divided at certain time intervals which are arbitrarily set, signals from the subscribers of the radio mobile station apparatuses 11 become discrete signals. It is inconvenient if the  
20 converted slot signals 202 as a result of the conversion can not be subjected to the despreading process at the correlation circuit at the discontinuities. Therefore, in this embodiment of the present invention, the following process is performed to allow the correlation circuit to  
25 perform the despreading in the same manner as performed on a continuous signal even at the discontinuities.

Specifically, in an example shown in Fig. 4, the reception signal 201 is divided into a reception signal F and a reception signal E. At this time, the signal is divided such that the reception signals E and F have an overlapping portion 201a. The divided signals E and F are in a configuration in which m signals similar to the divided signals are repeatedly located as apparent from the slot signal 202. "m" represents the number of the stages of the stage processing for canceling interference. The effect of interference cancellation becomes more significant, the greater the number of the stages. However, since the time required for the process increases with the number of the stages, a value optimum for the system is set in consideration to the effect of interference cancellation and the processing time.

Referring to the process at the interference canceller of the present embodiment, stage processing for canceling interference is carried out by performing a despreading process on a reception signal located in the first slot of a signal having a slot configuration and performing a despreading process on a feedback signal located in the second slot. A configuration is employed in which the gain of the stage processing on data obtained after the despreading process is improved by accumulating at each stage the despread signal obtained by despreading at each slot. The circuit for accumulating despread signals at each

stage of the stage processing has a configuration in which selector circuits are provided at a signal input/output portion to allow selection of signals to be added and signals to be transmitted to the subsequent stage. When only a small  
5 number of stages are sufficient because of reasons such as a small number of multiplexing, the number of the stages for stage processing can be changed by switching the selectors without changing the slot configuration. By selecting signals to be transmitted to the subsequent stage  
10 with the selectors, it is possible to select signals which can be used as modulation signals for generating replica signals.

A description will now be made with reference to Fig. 5 on the process at the above-described stages for canceling  
15 interference.

A signal which has been converted by the slot configuration circuit 103 into a signal 202 having a slot configuration is divided into two signals. One of the signals is inputted to the subtraction process circuit 122  
20 as it is in the slot configuration to perform the subtraction process. The other signal becomes a signal 301 selected by the selector 104 and is inputted to the correlation circuit 105. As shown in Fig. 5B, the signal 301 is has a signal only in the first slot. Thereafter, the signal  
25 which has passed through the selector 104 is subjected to the despreading process at the correlation circuit 105, the

re-spreading process at the re-spreading circuit 110, the  
 synthetic process at the synthesis circuit 111 and the  
 subtraction process at the subtraction process circuit 112.  
 The signal which has been subjected to the subtraction  
 5 process passes through the delay circuit 114 to be fed back  
 to the correlation circuit 105 again. As shown as a signal  
 302 in Fig. 5C, the fed back signal is located in the second,  
 third and subsequent slots.

The fed back signal is subjected to the despreading  
 10 process at the correlation circuit 105 again. The stage  
 processing circuit 115 performs a process of adding the  
 despread signals to the demodulated data in the slots. The  
 process of adding the despread signals will now be described  
 with reference to Figs. 6A and Fig. 6B.

15 As shown in Fig. 6A, the stage processing circuit 115  
 comprises the selector 401, the adder 402, the selector 403,  
 the delay circuit 404 and the selector 405. The adder 402  
 and delay circuit 404 accumulatively add a despread signal  
 inputted thereto with the despread signal in the preceding  
 20 slot. As a result, a signal obtained by accumulatively  
 adding thereto despread signals outputted by the stage  
 processing circuit 115 is as indicated by 406 in Fig. 6B.  
 The signal to which a multiplicity of despread signals have  
 been accumulatively added is a signal from which  
 25 interference has been canceled. Through a demodulation  
 process on such a signal, the signal is demodulated into

a signal from which interference has been canceled.

In the past, the number of the correlation circuits 105 has been required in the same quantity as the number of users for whom demodulation is to be carried out. This embodiment of the present invention has a configuration in which a plurality of user signals can be demodulated with a single correlation circuit using an elaborate method for signal processing. The configuration of the embodiment of the present invention makes it possible to decrease the number of correlation circuits which has conventionally increased with the number of users.

Reception signals inputted to the correlation circuit are inputted to a shift register and are sequentially shifted to subsequent shift registers. The correlation circuit multiplies the reception signals with codes for despreading and calculates the sum of the results of the multiplication to output a correlation value. It performs the process continuously to demodulate the signals. The codes for despreading are generated by the code generation circuit 108, and a code required for demodulating each user signal is separately generated. The generated despreading codes are set in the code setting elements of the correlation circuit to perform a demodulation process. The method of setting the codes is characteristic of the present invention.

Normally, the reception signals are different from

despre...ng codes in the number of de... stages of the shift registers, because the reception signals are oversampled. However, the reception signals and despreading codes are shifted to subsequent steps in synchronism with each other.

5 As a result, although they each have the identical reception signal to be inputted to the correlation circuit, the same number of the correlation circuits is necessary as that of users for whom demodulation is carried out, because a despreading code to be set is different among users. Under

10 such circumstances, the embodiment of the present invention employs a configuration in which the codes set in the code setting elements of the correlation circuit can be instantaneously switched within the time during which a reception signal is set in a shift register and is shifted

15 once to the subsequent shift register. This makes it possible to switch the setting of despreading codes for all user signals, thereby enabling a despreading process on a plurality of user signals. When a configuration is employed in which output of demodulated signals is also

20 instantaneously switched in synchronism with the switching of the codes to be set, correlation value signals obtained by detecting correlation between a plurality of users can be outputted concurrently. It is therefore possible to perform a despreading process on a plurality of user signals

25 with one correlation circuit.

A configuration and operation of the above-described



correlation circuit 105 will now be described with reference to Fig. 7.

The correlation circuit 105 comprises shift registers 501, desreading code setting elements 502, addition circuits 503 and selectors 504 as a matched filter 506. As is well known, since a signal obtained by converting the frequency of a reception signal into that of a baseband signal is divided into an I-axis signal and a Q-axis signal, two sets of the above-described configuration are provided as the matched filter 506. The matched filter 506 is connected to a code generator 108 for generating codes for setting desreading codes, a selector 107, and a control unit 505 for controlling the switching of the selector 107.

The code generator 108 generates on a user-by-user basis desreading codes for demodulation for demodulating the reception signal. Those desreading codes are sequentially switched at a high speed by the selectors 107 and are set in the spreading code setting elements 502. The control unit 505 controls the switching of the selectors 504 for switching the output of correlation values simultaneously with the switching of desreading code setting. The same number of signal lines as that of users for whom the desreading process can be performed are connected to the output side of the selectors 504. By switching the selectors 504, signals obtained after correlation value processing are concurrently outputted at

the output of the correlation circuit 105 in a quantity equivalent to the number of users for whom demodulation is to be performed.

The path detection circuit 106 used in the multi-stage interference canceller device in the present embodiment of the invention can detect paths using signals which has been correlation-detected and subjected to stage processing for canceling interference. Normally, synchronous process and path detection of reception signals, and path are performed at the beginning of reception, and a despreading process is performed based on the resultant data. In the case of a radio communication system based on the code division multiple access, however, fine power control is carried out between the base stations and mobile stations to control transmission power such that the SIR, i.e., the ratio between the power of transmission signal power and reception-interfering power is always maintained at a constant value. Therefore, when interference components are suppressed by an interference canceller, a power control signal is transmitted to a transmitter side for reducing the power. As a result, the power of reception signals gradually decreases. Since the interference suppressing effect of an interference canceller reduces the power of reception signals gradually, it becomes difficult to detect paths with only the synchronization process at the initial stage and the path detection circuit.

Under such circumstances, the path detection circuit 106 used in the embodiment of the present invention is configured to be able not only to perform synchronous process and path detection at the beginning of reception, with a normal path detection circuit but also to perform path detection from signals whose interference components have been suppressed by the interference canceller. Specifically, a path detection signal at the initial stage is used to perform a despreading process on the first signal in the first slot. A correlation value signal obtained by the despreading process on the signal in the first slot is used for the signal in the second slot. A correlation value signal obtained by adding the correlation value signal for the first slot and the correlation value signal for the second slot is used to perform the despreading process on the signal in the third slot. It is a correlation value signal at the first stage for interference cancellation which has been subjected to the interference cancellation process. Similarly, a correlation value signal at the second stage for interference cancellation which is obtained by adding the correlation value signals for the first, second and third slots is used for despreading the signal in the fourth slot. By repeating the same process, correlation value signals which have been subjected to the stage processing for interference cancellation can be used to detect paths for the subsequent slots. Such signals

which have been subjected to the stage processing for interference cancellation are stored in a memory and are used for averaging process with the data at the subsequent stages, which makes it possible to perform path detection which is resistant to phasing and which is more accurate.

A configuration and operation of the above-described path detection circuit 106 will now be described with reference to Fig. 8.

The path detection circuit 106 comprises selectors 601, averaging circuits 602, accumulation circuits 603, forgetful averaging circuits 604, a path detection/peak detection circuit 606 and despread signal detection circuits 605. In this circuit, two sets of above-described features are provided in association with I-axis signals and Q-axis signals except for the path detection/peak detection circuit 606. The selectors 601 selects required demodulation signals from among signals from the correlation circuit 105 and selects only pilot signal portions out of the demodulation signals. The averaging circuits 602 average pilot signals in one slot.

A correlation value signal of pilot signals which are averaged in each slot is accumulatively added by the accumulation circuits 603 with an averaged correlation value signal of each of the subsequent slots wherein a stage processing has been performed by the addition circuits to provide a correlation value signal which has been subjected

to stage processing for interference cancellation. The correlation value signal which has been subjected to stage processing for interference cancellation is averaged at the forgetful averaging circuits 604 with several correlation value signals which have been subjected to stage processing for interference cancellation. The path detection/peak detection circuit 606 uses the correlation value signal obtained through the stage processing for interference cancellation to detect paths for reception signals and detect a peak of a path for symbol demodulation. Based on information of paths whose peaks have been detected by the path detection/peak detection circuit 606, symbol demodulation data are extracted from correlation value data outputted by the correlation circuit 105.

Fig. 9 shows a process flow for eliminating interference component according to this embodiment. First, received is a signal transmitted by a mobile station. (S101) Then, the reception signal is divided at certain time intervals and the divided signal is converted into a signal at a faster cycle. The thus obtained signals are converted into a signal having a serial slot configuration and including as many signals identical to the thus obtained signals as the number of stages for stage processing. (S102) This signal having the slot configuration is processed for eliminating the interference component. Specifically, the signal having the slot configuration and a feedback signal

are despread, and the number of stage or stage processing is added to the despread signal obtained by the despreading process. Then, the signal obtained by the above stage addition process is re-spread and all of the spread signals  
5 obtained by the re-spread process is synthesized for generating replica signals. Between the replica signals and the reception signals, a subtraction process is carried out for generating the feedback signal, consequently outputting signals obtained after the stage addition  
10 process.

According to the above-described embodiment of the invention, signal processing is performed by providing feedback of signals which have been subjected to stage processing for interference cancellation. This is  
15 advantageous in that hardware which has been required in a quantity equivalent to the number of stages can be significantly reduced while allowing signal processing similar to conventional stage processing using cascade connection.

20 The above-described embodiment of the invention makes it possible to demodulate a plurality of user signals with a single correlation circuit by switching despreading codes at a high speed and by switching synchronization of outputs while the correlation circuit has been required in a  
25 quantity equivalent to the number of users for whom demodulation is to be performed. This is advantageous in

that the number of correlation circuits can be reduced.

Furthermore, the above-described embodiment of the invention is advantageous in that the interference cancellation process reduces the amount of interference of demodulation signals and in that paths for reception signals can be detected even when receiving power is reduced as a result of power control, thereby allowing a greater number of reception signals to be multiplexed.

#### EFFECTS OF THE INVENTION

As described above, in the base transceiver station apparatus simultaneously communicating with a plurality of mobile station apparatuses, the present invention controls scale-up of the apparatus due to the provision of interference suppressing function which suppresses mutual correlation interference caused by the increase of users. Further, in accordance with the present invention, obtainable is a low-cost communication system employing a code division multiple access, which prevents the reduction of channel utilization efficiency and enables a high-quality communication.